TWO GBPS QPSK MODEM

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ABSTRACT

A 2 Gbps QPSK modulator and demodulator were developed and BER performance was evaluated over a millimeter wave data channel. The error rate measurements taken with the breadboard equipment showed system performance to be less than 2 dB from theoretical at an error rate of 10^{-5}. Additionally, a second QPSK modulator was constructed and combined with the first to generate 4 Gbps QASK data for future evaluation.

Introduction

The continuing demand for communication satellites to provide data channels at increased rates has prompted an experimental program investigating multigigabit communications technology. The initial program objectives were to develop a broadband millimeter wave satellite channel, a 2 Gbps QPSK Modem, and to evaluate the bit error rate performance of the resulting system. Following the evaluation of this Modem, two QPSK modulators were combined to form a 4 Gbps QASK modulator.

System Configuration

A block diagram of the system is shown in Figure 1. It includes a QPSK modulator operating at a 15 GHz carrier frequency, and an upconverter which translates the signal to the millimeter (MM) wave region where it is passed through a single conversion transponder. The transponder translates the signal back to 15 GHz and provides filtering and amplification. Following the transponder, noise is added to the signal before it is phase detected, filtered and latched in the demodulator which includes both carrier and clock recovery phase locked loops. The recovered data is processed in error detectors to provide system bit error rate evaluation.

Data Source and Modulator

Two 1 Gbps data sources drive a quadrature pair of FET bi-phase modulators which operate on a 15 GHz carrier oscillator to form a 2 Gbps QPSK modulated signal at 15 GHz. The 1 Gbps data sources are each formed by multiplexing and latching the outputs of 500 Mbps PRN sequence generators.

The 500 Mbps PRN sequence generators are mechanized using Fairchild 11C06 "D" flip flops. Each generator produces a maximum length sequence of 511 bits and generates two suitable phases of the word which are multiplexed to generate the original 511 bit word at twice the bit rate, or 1 Gbps.

The multiplexers are each mechanized using three GaAs FET chips. Two of the FETs operate as switches and connect each of the two 500 MHz data streams to the output on alternate phases of a 500 MHz clock. The third FET amplifies the multiplexed signal to a level suitable for driving a latch consisting of Hughes GaAs logic gates. The latch is clocked by a 1 GHz clock and performs the function of reducing time and amplitude jitter caused by intersymbol interference.

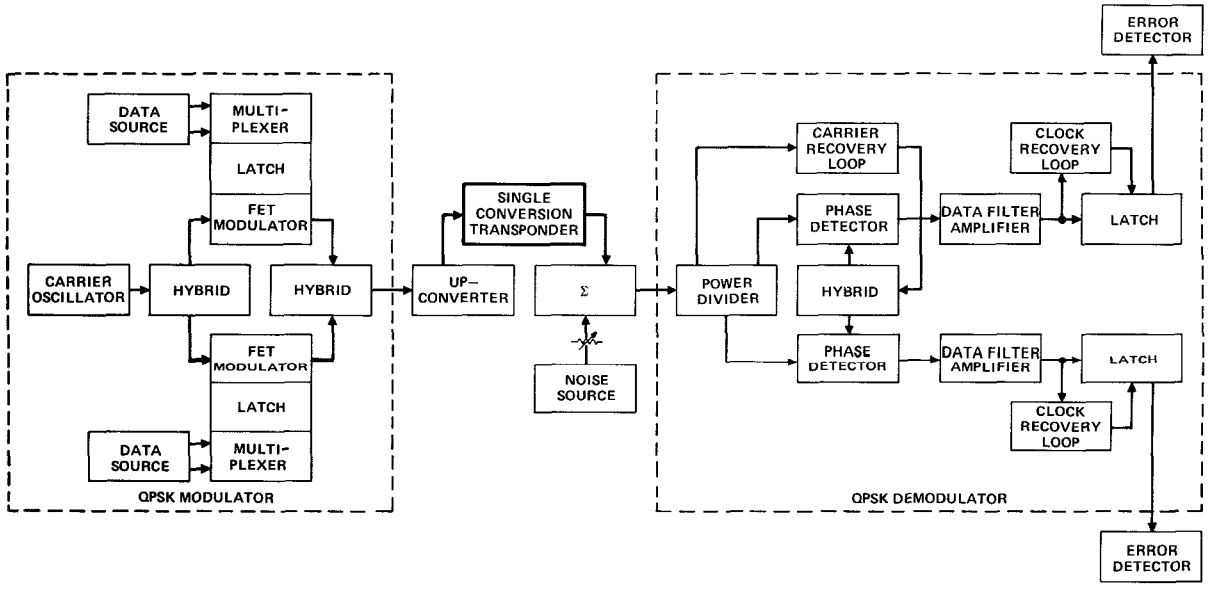


FIGURE 1. 2 GBPS SYSTEM BLOCK DIAGRAM

The outputs of the latches each drive a FET biphase modulator. The modulators each use a Ga As FET to switch the length of a waveguide stub in the signal path. The modulator switch and stub are coupled to the transmission path using a circulator. The use of a FET switch to apply the modulation provides a high quality modulated signal because of the low AM/PM limiting of the input data provided by the FET switch. Other advantages of the FET waveguide modulator configuration are its low DC power consumption, its inherent isolation between input data and output RF provided by the waveguide in the output signal path, and its potential for even higher data rates on MM wave carriers. The multiplexer latch and modulator are packaged in one compact assembly to minimize reflections between circuits. A photograph of the GaAs multiplexer, latch and modulator assembly is shown in Figure 2.

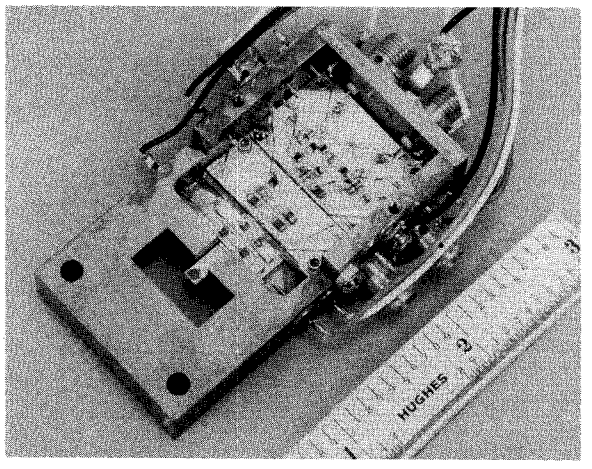


FIGURE 2. G_aA_s MULTIPLEXER – LATCH – MODULATOR ASSEMBLY

Demodulator

The input signal to the demodulator is divided into three paths. One path goes to the carrier recovery loop. The other two paths drive a quadrature pair of Airtech double balanced mixers which operate as phase detectors. Following the phase detectors the signals are passed through data filter amplifiers which increase the signal level, and provide post correlation data filtering. The output of each amplifier is sampled by a latch which is driven by a clock operating at one eighth the symbol rate. The reconstructed data emerges at 125 Mbps from each latch. This technique of undersampling the PRN data sequence allows BER evaluation using a conventional low speed BER test set.

Block diagrams of the carrier and clock recovery loops are shown in Figures 3 and 4. The carrier recovery circuit is an IQ loop, and the clock circuit consists of an edge detector followed by a phase locked loop. The clock circuit diagram illustrates the implementation of the one eighth rate clock to the latch.

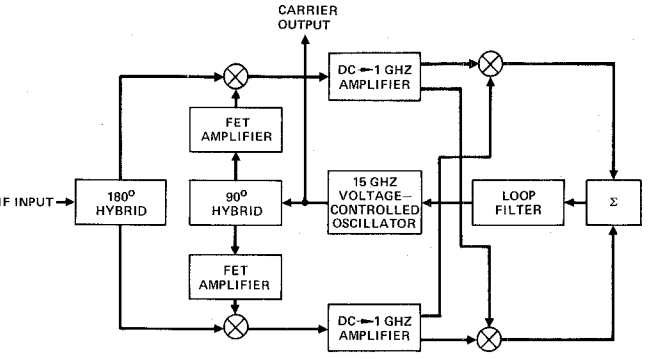


FIGURE 3. 2 GBPS QPSK CARRIER RECOVERY LOOP

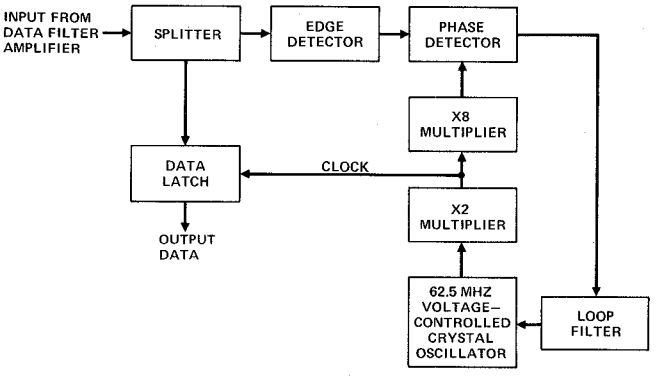


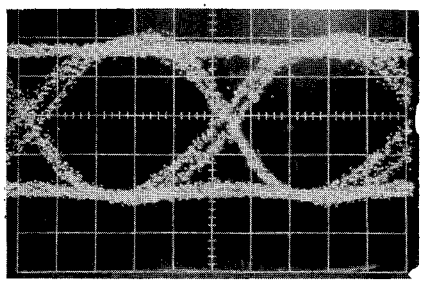
FIGURE 4. 2 GBPS QPSK CLOCK RECOVERY LOOP

Performance Evaluation

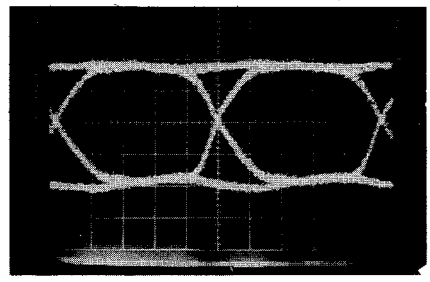
The high quality of the signals generated in the 2 Gbps system is demonstrated from waveform and spectrum photographs, as well as from a BER evaluation.

Figure 5 shows time and frequency domain displays taken at the multiplexer output, the latch output and the demodulator phase detector output. The first photograph shows the multiplexer output eye pattern. Timing jitter due to intersymbol interference is visible on this waveform. The second photograph is of an eye pattern taken at the latch output and shows the improvement in time and amplitude jitter. Figure (c) shows a segment of the PRN data sequence at the latch output. Note the single bit pulses of 1 nsec duration (print through at the 1 Ghz clock rate can also be seen as ripple on longer sequences of zeros or ones). Figure (d) is a frequency domain response of the same waveform and illustrates the near ideal (sin x)/x shape. The last two photographs were taken at the demodulator phase detector output with the transponder channel bypassed. Once again, they indicate the high quality of the waveforms encountered.

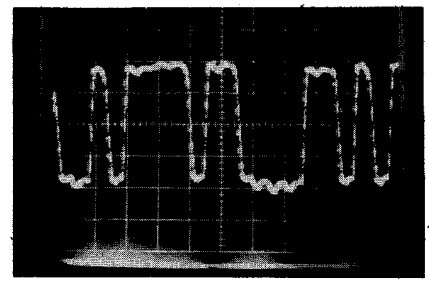
Bit error rate performance for the system is shown in Figure 6. The system was evaluated with the transponder bypassed (back-to-back) and with the transponder included. The measurements were taken with a strong signal into the transponder so that the preamplifier noise was negligible compared to the noise source (strong uplink, weak downlink). Degradation is approximately 2 dB with the transponder included. With the transponder bypassed, the degradation is slightly less.



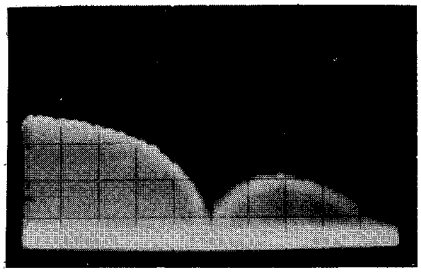
a) MULTIPLEXER OUTPUT 200 PSEC/CM



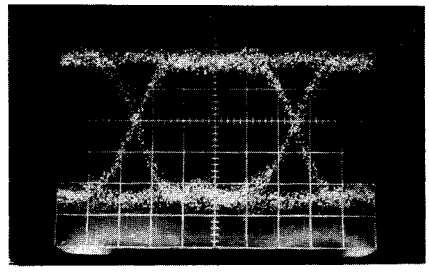
b) LATCH OUTPUT 200 PSEC/CM



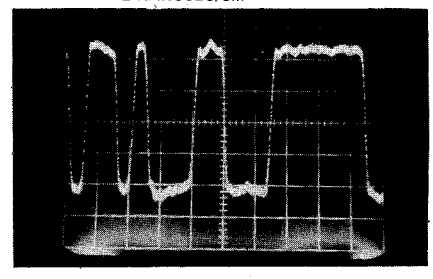
c) LATCH OUTPUT WAVEFORM
2 NANOSEC/CM



d) LATCH OUTPUT SPECTRUM
VERT. 10 db/CM HORIZ. 200 MHz/CM



e) DEMOD DETECTOR OUTPUT
200 PSEC/CM



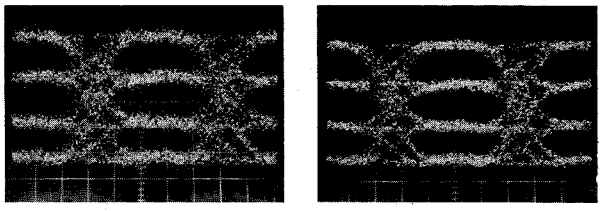
f) DEMOD DETECTOR OUTPUT
2 NANOSEC/CM

FIGURE 5. GPSK WAVEFORMS

4Gbps QASK Modulator

A second word generator, multiplexer, latch and modulator were constructed. This modulator and the original were driven with coherent carriers and their outputs were combined in a hybrid to form a 16 signal QASK modulator. A block diagram of the configuration, along with a vector construction of the signal set. is shown in Figure 7.

The QASK set of 16 signals has advantages in a high rate system because it provides twice the data rate without a bandwidth increase when compared with QPSK. Another advantage is that baseband circuits need only operate at half the speed required for QPSK. The disadvantages are that the signal set is approximately 4dB less power efficient than QPSK, that more hardware complexity is required, particularly in the receiving circuits, and that AM on the signal requires a linear, and, therefore, less efficient transmitter. An alternative to a linear transmitter is to locate saturating power amplifiers at the output of each QPSK modulator prior to the power combining hybrid. However, the required termination on the fourth port of the hybrid results in a 3dB power loss. Regardless of these difficulties, the bandwidth efficiency of this technique provides advantages for systems operating at the highest data rates. Demodulated eye pattern of the 4 Gbps QASK modulator is shown in Figure 8.



a) INPUT DATA ON I & Q

b) INPUT DATA ON I ONLY

FIGURE 8. 4GPBS QASK EYE PATTERNS

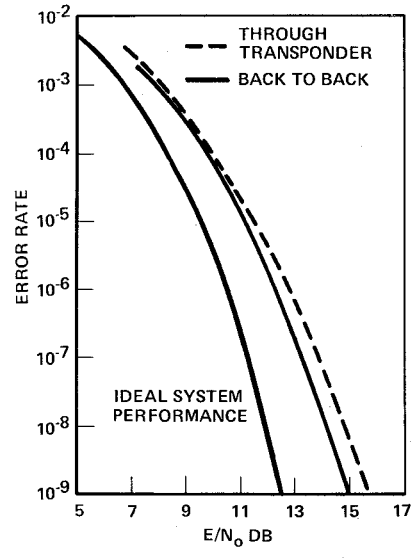


FIGURE 6. 2 GBIT SYSTEM BER PERFORMANCE

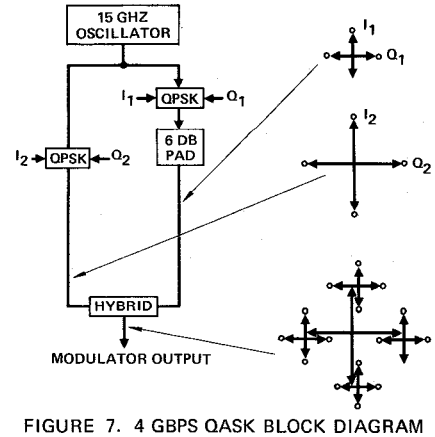


FIGURE 7. 4 GBPS QASK BLOCK DIAGRAM AND VECTOR CONSTRUCTION